REMARKS

The Office Action dated April 14, 2005, has been received and carefully considered. Reconsideration of the outstanding rejections in the present application is respectfully requested based on the following remarks.

I. THE ENABLEMENT REJECTION OF CLAIMS 1-39

On page 2 of the Office Action, claims 1-39 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. This rejection is hereby respectfully traversed.

The Examiner asserts that the term "common bus line" is new matter since the originally filed specification does not disclose a "common bus line." Applicant respectfully disagrees. Contrary to the Examiner's assertions, the original specification repeatedly discloses a common bus line, or conductor, over which devices that are coupled thereto simultaneously transmitting/receiving data, as claimed. For example, the specification discloses a bus topology that "allows more than two electrical circuits or devices to be coupled together along one or more common electrical conductors, with a bus comprising these one or more electrical conductors" (see page 5, lines 4-6). Also, the specification discloses that

"[d]evices 101, 102, 103, and 104 are coupled to bus 105. Bus 105 may include a single conductor or a plurality of conductors" (see Figure 1; page 7, lines 10-11). Furthermore, the specification discloses that "[i]n one embodiment, the bus comprises a conductor that operably couples the first memory device and the second memory device to the memory controller" (see page 11, lines 11-18). Additionally, in Figures 4-7, which the Examiner specifically refers to as NOT disclosing a common bus line, devices are coupled to a common bus line, or conductor (see page 13, line 5, to page 17, line 3). The Examiner is totally incorrect in his assertion that each of Figures 4-7 show more than one "common" bus line. For instance, the Examiner asserts that Figure 7 shows a common bus 703 having two bus lines 704 and 705. However, the specification clearly discloses that "[d]evice 701 is coupled to device 702 via conductor 703 in Figure 7 (see page 16, lines 23-24). Arrows 704 and 705 merely indicate the direction in which data is transmitted over conductor 703, and they are not separate bus lines as the Examiner asserts. Indeed, the specification only refers to conductor 703 in the singular, and never in the plural. (see page 16, line 24, to page 17, line 3). This is similarly the case in Figures 4-6. Interestingly, the Examiner acknowledges that a bus may be a collection of wires or lines over which data

is transmitted. Applicants wholeheartedly agree. Accordingly, it is respectfully submitted that the term "common bus line" is fully supported in the specification as being a single bus line, or conductor, over which devices that are coupled thereto simultaneously transmit/receive data, as claimed.

In view of the foregoing, it is respectfully requested that the aforementioned enablement rejection of claims 1-39 be withdrawn.

II. THE INDEFINITENESS REJECTION OF CLAIMS 1-39

On pages 2-3 of the Office Action, claims 1-39 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the invention. This rejection is hereby respectfully traversed.

As discussed above, the specification fully supports a clear and unambiguous meaning of the term "common bus line" as being a single bus line, or conductor, over which devices that are coupled thereto simultaneously transmit/receive data, as claimed.

In view of the foregoing, it is respectfully requested that the aforementioned indefiniteness rejection of claims 1-39 be withdrawn.

III. THE ANTICIPATION REJECTION OF CLAIMS 1-14 AND 17-39

On pages 3-6 of the Office Action, claims 1-14 and 17-39 were rejected under 35 U.S.C. § 102(e) as being anticipated by Garlepp et al. (U.S. Patent No. 6,687,780). This rejection is hereby respectfully traversed.

Under 35 U.S.C. § 102, the Patent Office bears the burden of presenting at least a prima facie case of anticipation. In re Sun, 31 USPQ2d 1451, 1453 (Fed. Cir. 1993) (unpublished). Anticipation requires that a prior art reference disclose, either expressly or under the principles of inherency, each and every element of the claimed invention. Id.. "In addition, the prior art reference must be enabling." Akzo N.V. v. U.S. International Trade Commission, 808 F.2d 1471, 1479, 1 USPQ2d 1241, 1245 (Fed. Cir. 1986), cert. denied, 482 U.S. 909 (1987). That is, the prior art reference must sufficiently describe the claimed invention so as to have placed the public in possession of it. In re Donohue, 766 F.2d 531, 533, 226 USPQ 619, 621 (Fed. Cir. 1985). "Such possession is effected if one of ordinary skill in the art could have combined the publication's description of the invention with his own knowledge to make the claimed invention." Id..

Regarding claims 1, 6, 10, 17, 24, 28, 33, and 39, the Examiner asserts that Garlepp et al. discloses the present invention as claimed. Specifically, the Examiner asserts that Garlepp et al. discloses a system providing simultaneous bidirectional signaling using a bus topology comprising: a first device (256) operably coupled to a bus (252, 254); a second device (262-1) operably coupled to the bus, the first device (256) transmitting a first portion of a first set of data to the second device (262-1) and the second device (262-1) transmitting a second portion of the first set of data to the first device (256) simultaneously during a first exchange slot; and a third device (262-2) operably coupled to the bus, the first device (256) transmitting a first portion of a second set of data to the third device (262-2) and the third device (262-2) transmitting a second portion of the second set of data to the first device (256) simultaneously during a second exchange slot.

However, it is respectfully submitted that Garlepp et al. fails to disclose, or even suggest, either alone or in combination with the other cited references, a method for providing simultaneous bidirectional signaling in a bus topology comprising the steps of: selecting a first memory device and a second memory device from among a plurality of memory devices coupled to a common bus line to exchange a first set of data;

scheduling a first exchange slot over which the first memory device and the second memory device are to exchange the first set of data; and during the first exchange slot, simultaneously transmitting a first portion of the first set of data from the first memory device to the second memory device over the common bus line and transmitting a second portion of the first set of the data from the second device to the first device over the common bus line, as recited in claim 1.

It is also respectfully submitted that Garlepp et al. fails to disclose, or even suggest, either alone or in combination with the other cited references, a system for providing simultaneous bidirectional signaling in a bus topology comprising: a first memory device coupled to a bus line; a second memory device coupled to the bus line, the first memory device transmitting a first portion of a first set of data over the bus line to the second memory device and the second memory device transmitting a second portion of the first set of data over the bus line to the first memory device simultaneously during a first exchange slot; and a third memory device coupled to the bus line, the first memory device transmitting a first portion of a second set of data over the bus line to the third memory device and the third memory device transmitting a second portion of the second set of data over the bus line to the first

memory device simultaneously during a second exchange slot, as recited in claim 6.

It is further respectfully submitted that Garlepp et al. fails to disclose, or even suggest, either alone or in combination with the other cited references, a memory device coupled to a bus line in a bus topology for providing simultaneous bidirectional signaling comprising: a transmitter circuit configured to provide additive signaling, the transmitter circuit applying transmit signals to the bus line; a receiver circuit operably coupled to the transmitter circuit, the receiver circuit configured to effectively subtract the transmit signals to receive received signals from the bus line, the transmitter circuit and the receiver circuit operating during an exchange slot, as recited in claim 10.

It is still further respectfully submitted that Garlepp et al. fails to disclose, or even suggest, either alone or in combination with the other cited references, a memory system comprising: a memory controller; a bus line coupled to the memory controller; a first memory device coupled to the bus line, the first memory device configured to simultaneously send first read data to the memory controller via the bus line and receive first write data from the memory controller via the bus line; and a second memory device coupled to the bus line, the

second memory device configured to simultaneously send second read data to the memory controller via the bus line and receive second write data from the memory controller via the bus line, as recited in claim 17.

It is still further respectfully submitted that Garlepp et al. fails to disclose, or even suggest, either alone or in combination with the other cited references, a memory device comprising: a transmitter circuit configured to drive a bus line with read data during an exchange slot while write data is present on the bus line; a receiver circuit operably coupled to the transmitter circuit, the receiver circuit configured to receive the write data from the bus line during the exchange slot while the transmitter circuit is driving the bus line with the read data; and a memory circuit operably coupled to the transmitter circuit and the receiver circuit, the memory circuit configured to provide the read data and to store the write data, as recited in claim 24.

It is still further respectfully submitted that Garlepp et al. fails to disclose, or even suggest, either alone or in combination with the other cited references, a memory controller comprising: a transmitter circuit configured to drive a bus line with first write data destined for a first memory device during a first exchange slot while first read data from the first

memory device is present on the bus line; a receiver circuit operably coupled to the transmitter circuit, the receiver circuit configured to receive the first read data from the bus line during the first exchange slot while the transmitter circuit is driving the bus line with the first write data, as recited in claim 28.

It is still further respectfully submitted that Garlepp et al. fails to disclose, or even suggest, either alone or in combination with the other cited references, a method for providing simultaneous bidirectional communication between a memory controller and a plurality of memory devices comprising the steps of: during a first exchange slot, simultaneously communicating over a common bus line first write data from the memory controller to a first memory device of the plurality of memory devices and first read data from the first memory device to the memory controller; and during a second exchange slot, simultaneously communicating over the common bus line second write data from the memory controller to a second memory device of the plurality of memory devices and second read data from the second memory device to the memory controller, as recited in claim 33.

It is still further respectfully submitted that Garlepp et al. fails to disclose, or even suggest, either alone or in

combination with the other cited references, a system for bidirectional communication of data over a common bus line comprising: a first device operably coupled to the common bus line, the first device comprising a first-to-second transmit buffer to hold first-to-second data and a first-to-third transmit buffer to hold first-to-third data; a second device operably coupled to the common bus line, the second device comprising a second-to-first transmit buffer to hold second-to-first data; a third device operably coupled to the common bus line, the third device comprising a third-to-first transmit buffer to hold third-to-first data; and a scheduler operably coupled to the common bus line, the scheduler scheduling the first device to transmit the first-to-second data and the second device to transmit the second-to-first data over the common bus line simultaneously during a first exchange slot and scheduling the first device to transmit the first-to-third data and the third device to transmit the third-to-first data over the common bus line simultaneously during a second exchange slot, the scheduler introducing a turnaround delay sufficient to prevent inter-symbol interferences between the first exchange slot and the second exchange slot, as recited in claim 39.

Claims 2-5 are dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed

above, claims 2-5 should also be allowable at least by virtue of their dependency on independent claim 1. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination, as Applicant has previously discussed.

Claims 7-9 are dependent upon independent claim 6. Thus, since independent claim 6 should be allowable as discussed above, claims 7-9 should also be allowable at least by virtue of their dependency on independent claim 6. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination, as Applicant has previously discussed.

Claims 11-14 are dependent upon independent claim 10. Thus, since independent claim 10 should be allowable as discussed above, claims 11-14 should also be allowable at least by virtue of their dependency on independent claim 10. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination, as Applicant has previously discussed.

Claims 18-23 are dependent upon independent claim 17. Thus, since independent claim 17 should be allowable as discussed above, claims 18-23 should also be allowable at least

by virtue of their dependency on independent claim 17. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination, as Applicant has previously discussed.

Claims 25-27 are dependent upon independent claim 24. Thus, since independent claim 24 should be allowable as discussed above, claims 25-27 should also be allowable at least by virtue of their dependency on independent claim 24. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination, as Applicant has previously discussed.

Claims 29-32 are dependent upon independent claim 28. Thus, since independent claim 28 should be allowable as discussed above, claims 29-32 should also be allowable at least by virtue of their dependency on independent claim 28. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination, as Applicant has previously discussed.

Claims 34-38 are dependent upon independent claim 33. Thus, since independent claim 33 should be allowable as

discussed above, claims 34-38 should also be allowable at least by virtue of their dependency on independent claim 33. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination, as Applicant has previously discussed.

At this point it should be noted that (1) the present application and Garlepp et al. have a common inventor, Frederick A. Ware, and (2) the present application and Garlepp et al. are commonly owned. Thus, Applicant reserves the right to swear behind the filing date of Garlepp et al. under a 37 C.F.R. § 1.131 Declaration. While Applicant retains the right to perform this action, it is believed that Garlepp et al. fails to disclose the claimed invention as discussed above.

In view of the foregoing, it is respectfully requested that the aforementioned anticipation rejection of claims 1-14 and 17-39 be withdrawn.

IV. CONCLUSION

In view of the foregoing, it is respectfully submitted that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by

telephone at the below listed telephone number, in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

To the extent necessary, a petition for an extension of time under 37 CFR § 1.136 is hereby made.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-0206, and please credit any excess fees to the same deposit account.

Respectfully submitted,

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APPENDIX A

1 (Previously Presented). A method for providing simultaneous bidirectional signaling in a bus topology comprising the steps of:

selecting a first memory device and a second memory device from among a plurality of memory devices coupled to a common bus line to exchange a first set of data;

scheduling a first exchange slot over which the first memory device and the second memory device are to exchange the first set of data; and

during the first exchange slot, simultaneously transmitting a first portion of the first set of data from the first memory device to the second memory device over the common bus line and transmitting a second portion of the first set of the data from the second device to the first device over the common bus line.

2 (Previously Presented). The method of claim 1 further comprising the steps of:

selecting the first memory device and a third memory device to exchange a second set of data;

scheduling a second exchange slot over which the first memory device and the third memory device are to exchange the second set of data; and

during the second exchange slot, simultaneously transmitting a first portion of the second set of data from the first memory device to the third memory device over the common bus line and transmitting a second portion of the second set of the data from the third memory device to the first memory device over the common bus line.

3 (Original). The method of claim 2 further comprising the step of:

introducing a turnaround delay between the first exchange slot and the second exchange slot.

4 (Previously Presented). The method of claim 3 wherein the turnaround delay is less than twice an end-to-end propagation delay of the common bus line.

5 (Previously Presented). The method of claim 1 wherein the first memory device is a memory controller device, and the second memory device is a memory storage device and wherein the first portion of the first set of data and the first portion of the second set of data are write data and the second portion of the first set of data and the second portion of the second set of data are read data.

6 (Previously Presented). A system for providing simultaneous bidirectional signaling in a bus topology, the system comprising:

a first memory device coupled to a bus line;

a second memory device coupled to the bus line, the first memory device transmitting a first portion of a first set of data over the bus line to the second memory device and the second memory device transmitting a second portion of the first set of data over the bus line to the first memory device simultaneously during a first exchange slot; and

a third memory device coupled to the bus line, the first memory device transmitting a first portion of a second set of data over the bus line to the third memory device and the third memory device transmitting a second portion of the second set of data over the bus line to the first memory device simultaneously during a second exchange slot.

7 (Original). The system of claim 6 wherein a turnaround delay exists between the first exchange slot and the second exchange slot.

8 (Previously Presented). The system of claim 7 wherein the

turnaround delay is less than twice an end-to-end propagation delay associated with the bus line.

9 (Previously Presented). The system of claim 6 wherein the first memory device is a memory controller device, and the second memory device is a memory storage device and wherein the first portion of the first set of data and the first portion of the second set of data are write data and the second portion of the first set of data and the second portion of the second set of data are read data.

10 (Previously Presented). A memory device coupled to a bus line in a bus topology for providing simultaneous bidirectional signaling, the memory device comprising:

a transmitter circuit configured to provide additive signaling, the transmitter circuit applying transmit signals to the bus line;

a receiver circuit operably coupled to the transmitter circuit, the receiver circuit configured to effectively subtract the transmit signals to receive received signals from the bus line, the transmitter circuit and the receiver circuit operating during an exchange slot.

11 (Previously Presented). The memory device of claim 10 wherein the memory device is coupled to the bus line by an impedance-matching splitter.

12 (Previously Presented). The memory device of claim 10 wherein the memory device further comprises:

a terminator operably coupled to the transmitter circuit and the receiver circuit, the terminator providing a controlled termination impedance.

13 (Previously Presented). The memory device of claim 10 wherein the transmitter circuit further comprises:

a driver operably coupled to the bus line, the driver configured to apply the transmit signals to the bus line using additive signaling; and

a transmitter operably coupled to the driver, the transmitter providing the transmit signals to the driver.

14 (Previously Presented). The memory device of claim 13 wherein the transmitter circuit further comprises:

a plurality of transmit buffers operably coupled to the transmitter, the plurality of transmit buffers configured to hold data destined for different other memory devices.

15 (Previously Presented). The memory device of claim 13 wherein the receiver circuit further comprises:

a comparator operably coupled to the transmitter, the driver, and the bus line, the comparator configured to effectively subtract the transmit signals to yield received signals from the bus line; and

a receiver operably coupled to the comparator, the receiver receiving the received signals and obtaining received data from the received signals.

16 (Previously Presented). The memory device of claim 15 further comprising:

an enabling circuit, coupled to the transmit circuit and the receive circuit, responsive to an exchange slot indication, the enabling circuit enabling the operation of the transmit circuit and the receive circuit during the exchange slot.

17 (Previously Presented). A memory system comprising:

a memory controller;

a bus line coupled to the memory controller;

a first memory device coupled to the bus line, the first memory device configured to simultaneously send first read data

to the memory controller via the bus line and receive first write data from the memory controller via the bus line; and

a second memory device coupled to the bus line, the second memory device configured to simultaneously send second read data to the memory controller via the bus line and receive second write data from the memory controller via the bus line.

18 (Previously Presented). The memory system of claim 17 wherein the first memory device is configured to simultaneously send the first read data to the memory controller and receive the first write data from the memory controller during a first exchange slot and wherein the second memory device is configured to simultaneously send the second read data to the memory controller and receive the second write data from the memory controller during a second exchange slot.

19 (Original). The memory system of claim 18 wherein the memory controller comprises:

a first write buffer to hold the first write data pending arrival of the first exchange slot.

20 (Original). The memory system of claim 19 wherein the memory controller comprises:

a second write buffer to hold the second write data pending arrival of the second exchange slot.

21 (Previously Presented). The memory system of claim 17 wherein the bus line comprises:

a conductor coupling the first memory device and the second memory device to the memory controller, wherein the first memory device is configured to simultaneously send a first read bit of the first read data to the memory controller over the conductor and receive a first write bit of the first write data from the memory controller over the conductor during a first exchange slot and wherein the second memory device is configured to simultaneously send a second read bit of the second read data to the memory controller over the conductor and receive a second write bit of the second write data from the memory controller over the conductor during a second exchange slot.

22 (Original). The memory system of claim 21 wherein a turnaround delay sufficient to prevent inter-symbol interference is introduced between the first exchange slot and the second exchange slot.

23 (Original). The memory system of claim 17 wherein the memory

controller performs coherency checking during memory access operations.

24 (Previously Presented). A memory device comprising:

a transmitter circuit configured to drive a bus line with read data during an exchange slot while write data is present on the bus line;

a receiver circuit operably coupled to the transmitter circuit, the receiver circuit configured to receive the write data from the bus line during the exchange slot while the transmitter circuit is driving the bus line with the read data; and

a memory circuit operably coupled to the transmitter circuit and the receiver circuit, the memory circuit configured to provide the read data and to store the write data.

25 (Previously Presented). The memory device of claim 24 further comprising:

an enabling circuit responsive to an exchange slot indication, the enabling circuit operably coupled to the transmitter circuit and the receiver circuit, the enabling circuit enabling interaction of the transmitter circuit and the receiver circuit with the bus line during the exchange slot.

26 (Previously Presented). The memory device of claim 25 wherein the enabling circuit is configured to be responsive to the exchange slot indication following a turnaround delay sufficient to prevent inter-symbol interference.

27 (Previously Presented). The memory device of claim 24 wherein the transmitter circuit further comprises:

a driver operably coupled to the bus line, the driver configured to drive the bus lines with the read data using additive signaling;

a transmitter operably coupled to the driver, the transmitter providing the read data to the driver; and

a transmit buffer operably coupled to the transmitter, the transmit buffer holding the read data pending arrival of the exchange slot.

28 (Previously Presented). A memory controller comprising:

a transmitter circuit configured to drive a bus line with first write data destined for a first memory device during a first exchange slot while first read data from the first memory device is present on the bus line; and

a receiver circuit operably coupled to the transmitter

circuit, the receiver circuit configured to receive the first read data from the bus line during the first exchange slot while the transmitter circuit is driving the bus line with the first write data.

29 (Previously Presented). The memory controller of claim 28 wherein the transmitter circuit is further configured to drive the bus line with second write data destined for a second memory device during a second exchange slot while second read data from the second memory device is present on the bus line and wherein the receiver circuit is further configured to receive the second read data from the bus line during the second exchange slot while the transmitter circuit is driving the bus line with the second write data.

30 (Original). The memory controller of claim 29 wherein a turnaround delay sufficient to prevent inter-symbol interference is introduced between the first exchange slot and the second exchange slot.

31 (Previously Amended). The memory controller of claim 28 wherein the transmitter circuit further comprises:

a driver operably coupled to the bus line, the driver

configured to drive the bus line with the first write data using additive signaling; and

a transmitter operably coupled to the driver to transmit the first write data to the driver.

32 (Previously Presented). The memory controller of claim 31 wherein the transmitter circuit further comprises:

a first transmit buffer to hold the first write data pending arrival of the first exchange slot; and

a second transmit buffer to hold the second write data pending arrival of the second exchange slot.

33 (Previously Presented). A method for providing simultaneous bidirectional communication between a memory controller and a plurality of memory devices comprising the steps of:

during a first exchange slot, simultaneously communicating over a common bus line first write data from the memory controller to a first memory device of the plurality of memory devices and first read data from the first memory device to the memory controller; and

during a second exchange slot, simultaneously communicating over the common bus line second write data from the memory

controller to a second memory device of the plurality of memory devices and second read data from the second memory device to the memory controller.

34 (Original). The method of claim 33 further comprising the step of:

holding the first write data destined for the first memory device in the memory controller pending arrival of the first exchange slot.

35 (Original). The method of claim 34 further comprising the step of:

holding the second write data destined for the second memory device in the memory controller pending arrival of the second exchange slot.

36 (Original). The method of claim 35 wherein the step of holding the first write data occurs in a first write buffer and wherein the step of holding the second write data occurs in a second write buffer.

37 (Original). The method of claim 35 further comprising the steps of:

holding the first read data destined for the memory controller in the first memory device; and

holding the second read data destined for the memory controller in the second memory device.

38 (Previously Presented). The method of claim 37 wherein the step of simultaneously communicating over the common bus line the first write data from the memory controller to the first memory device and the first read data from the first memory device to the memory controller occurs after a specified amount of the first write data destined for the first memory device is held in the memory controller.

39 (Previously Presented). A system for bidirectional communication of data over a common bus line comprising:

a first device operably coupled to the common bus line, the first device comprising a first-to-second transmit buffer to hold first-to-second data and a first-to-third transmit buffer to hold first-to-third data;

a second device operably coupled to the common bus line, the second device comprising a second-to-first transmit buffer to hold second-to-first data;

a third device operably coupled to the common bus line, the

third device comprising a third-to-first transmit buffer to hold third-to-first data; and

a scheduler operably coupled to the common bus line, the scheduler scheduling the first device to transmit the first-to-second data and the second device to transmit the second-to-first data over the common bus line simultaneously during a first exchange slot and scheduling the first device to transmit the first-to-third data and the third device to transmit the third-to-first data over the common bus line simultaneously during a second exchange slot, the scheduler introducing a turnaround delay sufficient to prevent inter-symbol interferences between the first exchange slot and the second exchange slot.